The opinion in support of the decision being entered today was not written for publication in a law journal and is not binding precedent of the Board.

Paper No. 38

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CONSTANTIN BULUCEA
and
REBECCA ROSSEN

Appeal No. 2000-1483
Application No. 08/851,608

ON BRIEF

Before HAIRSTON, KRASS and RUGGIERO, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 17-21, 25-37, 39-41, 44, 46-58, 60-62, 64 and 65. Claims 22, 23, 38, 42, 59 and 63 have been indicated by the examiner as being allowable and are not before us on appeal. No other claims are pending.

The invention is directed to a trench DMOS transistor cell. The gate region is positioned in the trench "that extends from the top surface of the structure downward, using a three-dimensional cell geometry that maximizes the gate dielectric breakdown voltage and also provides position of voltage breakdown initiation to allow use of controlled bulk semiconductor breakdown" (specification, page 2).

Representative independent claim 17 is reproduced as follows:

17. A trench DMOS transistor cell, comprising:

a substrate of a first conductivity type, said substrate having a surface;

an epitaxial layer of said first conductivity type formed on said surface of said substrate, said epitaxial layer having a top surface and a bottom surface, said epitaxial layer having a substantially uniform initial dopant concentration at formation;

a body region of a second conductivity type formed in said epitaxial layer, said body region extending, as measured from said top surface of said epitaxial layer, to a first depth d_{max} at a first location and to a depth of d at a second location, where d is less than d_{max}, said first and second locations being separated by a predetermined horizontal distance;

a source region of said first conductivity type formed in said expitaxial [sic] layer above a portion of said body region, said portion of said body region being located between said second location and said source region; and

a trench formed in said epitaxial layer, having substantially vertical side walls, extending from said top surface of said epitaxial layer to a depth d_{tr}, said depth d_{tr} being less than said depth d_{max}, and greater than said depth d, said trench being (i) closer to said second location than said first location, and (ii) horizontally adjacent said source region;

wherein breakdown in said trench DMOS transistor occurs across said epitaxial layer at a position closer to said first location than said second location.

The examiner relies on the following references:

Jambotkar	4,165,700	Mar. 20, 1979
Tonnel	4,420,379	Dec. 13, 1983

Daisuke Ueda et al. (Ueda), "A New Vertical Power MOSFET Structure with Extremely Reduced On-Resistance," ED-32 IEEE Transactions on Electron Devices no. 1, 2-6 (January 1985)

Kikuo Yamabe et al. (Yamabe), "Nonplanar Oxidation and Reduction of Oxide Leakage Currents at Silicon Corners by Rounding-off Oxidation," ED-34 IEEE Transactions on Electron Devices no. 8, 1681-87 (August 1987)

Claims 17-21, 25-37, 39-41, 44, 46-58, 60-62, 64 and 65 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner offers Tonnel and Ueda with regard to claims 17-21, 25-29, 32-37, 44, 46-58, 64 and 65, adding Jambotkar with regard to claim 30 and further adding Yamabe with regard to claims 31, 39-41 and 60-62.

Reference is made to the brief and answer for the respective positions of appellants and the examiner.

OPINION

At the outset, we note that many of appellants' arguments in the brief are moot in view of the examiner's withdrawal of any reliance on the Lidow, Hendrickson, Bulucea and Lisiak references. The examiner has also withdrawn a rejection based on obviousness-type double patenting in view of appellants' terminal disclaimer.

It is the examiner's position, with regard to claim 17, that Tonnel, taken together with Ueda, suggests a trench having vertical side walls (i.e., U-shaped) and that Figure 3 of Tonnel discloses a DMOS transistor cell that comprises an N-type substrate 20, a uniformly doped N-type epitaxial layer 21 with a finite thickness formed on the substrate, trench 30, a P-type body region 25 having a depth at a second location less than the trench slot depth, with N-type source regions 26 formed above the body region in the second location horizontally adjacent the trench slots. The examiner goes on to state that the P-type guard ring body portion 22 is "formed substantially more deep than the trench slot depth; whereby a lateral distance between the trench slot (30) and the P-type body region portion (25) at a second location was substantially less than a distance between

the trench slot (30) and the guard ring body portion at a first location (22)" (answer, paragraph bridging pages 5 and 6).

In Figure 3 of Tonnel, guard ring body portion 22 is clearly not deeper than trench 30, so the examiner relies on other Figures within Tonnel, e.g., Figure 12, to show successive stages in the manufacture of the Figure 3 device, wherein the guard ring body portion is clearly deeper than the trench.

Based on the examiner's combination of Tonnel and Ueda and the examiner's interpretation of Tonnel, the examiner concludes that:

> [O]ne also would have readily achieved the claimed property that transistor breakdown occurred across the epitaxial layer closer to the first location than to the second location, because the claimed property itself would have constituted a property inherent in the prior art trench (slot) DMOS transistor . . . a newly discovered property inherently possessed by things in the prior art does not cause a Claim drawn to those things to distinguish over the prior art, after at least *In re Swinehart*, [439 F.2d 210,] 169 USPQ 226 (CCPA 1971); *In re Best*, [562 F.2d 1252,] 7195 USPQ 430 (CCPA 1977) [answer, page 6].

Appellants do not dispute the examiner's allegation of the obviousness of making Tonnel's V-shaped trench a U-shaped trench having vertical side walls in view of Ueda.

With regard to Figures 10-12 of Tonnel, appellants do not deny that these Figures depict a P-type region 22 being drawn

deeper into the substrate 21 than V-slots 31. Appellants argue merely that there is "no corresponding verbal teaching in Tonnel's specification regarding this spatial relationship between V-slots 31 and P-type region 22" (brief, page 6). Thus, appellants conclude that the examiner's rationale is based on hindsight and speculation and urge that such "speculation and hindsight reconstruction cannot supplement the absence of teaching in Tonnel regarding the spatial relationship discussed above and recited in Applicants' claims" (brief, page 6).

Merely because Tonnel does not verbally teach the spatial relationship between V-slots 31 and P-type region 22, this does not vitiate the clear teaching of what is shown in Tonnel's Figures 10-12 regarding the claimed spatial relationship. Appellants do not dispute what is shown in these Figures of Tonnel nor do appellants offer any other explanation of what is shown by Tonnel and how the claimed structure distinguishes thereover. The examiner is not speculating if the Figures of the reference show the claimed structure.

Appellants further argue that claim 17 recites a limitation, viz., "wherein breakdown in said trench DMOS transistor occurs across said epitaxial layer at a position closer to said first location than said second location," which results from the

claimed spatial relationship and that this is neither disclosed nor suggested by the applied references.

The examiner never suggested that this claim limitation was disclosed or suggested by Tonnel. Rather, the examiner is alleging that since the structure is shown by Tonnel or would have been suggested by the combination of Tonnel and Ueda, the resulting structure, being the same as that claimed, would have resulted in the claimed limitation regarding the breakdown in the trench being "inherent" in that structure.

In our view, the examiner makes a valid point in asserting that a newly discovered property inherently possessed by things in the prior art does not cause a claim drawn to those things to distinguish over the prior art. However, in the instant case, one cannot say that the instant claimed structure and the structure resulting from the combination of Tonnel and Ueda are identical.

While the broad spatial relationship between d_{tr}, d_{max}, and d may be shown by Tonnel, in Figures 10-12, it is not merely that d_{tr} be less than d_{max} and greater than d. This much is shown by Tonnel. Claim 17 also requires that these relationships be such that "breakdown in said trench DMOS transistor occurs across said epitaxial layer at a position closer to said first location than

said second location." Thus, there must be a certain combination of the relative distances d_{tr}, d_{max}, and d such that this limitation will occur. Since no such specific relationship is disclosed by Tonnel, it cannot be said, with certainty, that this limitation, i.e., wherein breakdown in said trench DMOS transistor occurs across said epitaxial layer at a position closer to said first location than said second location, will inherently occur in Tonnel.

This is made more specific in claims such as claim 20, wherein d_{tr} is less than d_{max} "by an amount sufficient to cause semiconductor surface breakdown to occur at a location closer to said first location than to said second location," or claim 21 which specifies the thickness of the epitaxial layer so as "to cause semiconductor surface breakdown to occur at a location closer to said first location than said second location."

Accordingly, we will not sustain the rejection of claim 17, or of claims 18-21 and 25-29, dependent thereon, under 35 U.S.C. § 103.

Similarly, independent claim 30 sets forth a spatial relationship of depths d_1 and d_2 and recites, "wherein junction breakdown occurs away from the trench and into a portion of the second covering layer." Since there is no evidence that Tonnel,

Ueda or Jambotkar performs such a function, and it cannot be said that this function is inherent, because it only comes about through a specific combination of depths, we will not sustain the rejection of claim 30 under 35 U.S.C. § 103, or of claim 31 which depends therefrom (since Yamabe does not provide for the deficiencies of the other references).

Similarly, independent claims 32, 46, 52 and 54, as well as the claims dependent thereon, contain equivalent limitations regarding recitations of various spatial relationships between depths and distances and how such relationships result in junction breakdown, or avalanche breakdown occurring away from the trench and how there is a reverse bias around the breakdown voltage (claim 52). Since this is not inherent in the structure of the references, and certainly not explicitly suggested therein, we will not sustain the rejection of any of these claims under 35 U.S.C. § 103.

The examiner's decision rejecting claims 17-21, 25-37, 39-41, 44, 46-58, 60-62, 64 and 65 under 35 U.S.C. § 103 is reversed.

REVERSED

KENNETH W. HAIRSTON)
Administrative Patent Judge)
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ERROL A. KRASS) BOARD OF PATENT
Administrative Patent Judge) APPEALS AND
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